What is claimed is:

1. A method for forming a semiconductor device, comprising:

forming a first conductive layer and at least one dielectric layer on the first conductive layer;

forming a patterned mask layer over the at least one dielectric layer and overlying the first conductive layer;

etching the at least one dielectric layer and the first conductive layer using the mask as a pattern to form first and second cross-sectional sidewalls from the at least one dielectric layer and the first conductive layer;

forming a first dielectric spacer on the first sidewall and a second dielectric spacer on the second sidewall, where an upper surface of each sidewall is above an upper surface of the first and second spacers;

forming a second conductive layer over the at least one dielectric layer and over the first conductive layer;

removing the second conductive layer from over the first conductive layer and leaving the second conductive layer at other locations;

etching the at least one dielectric layer to expose the first conductive layer; then

forming a silicide layer simultaneously on the first and second conductive layers.

2. The method of claim 1 wherein the etching of the at least one dielectric layer to expose the first conductive layer is performed in the absence of a mask.

3. The method of claim 1 wherein the etch of the first conductive layer defines a plurality of transistor control gates.

4. The method of claim 3 wherein the removal of the second conductive layer from over the first conductive layer defines a plurality of conductive plugs which contact a semiconductor wafer.

5. The method of claim 1 wherein the formation of the at least one dielectric layer comprises:

forming a first silicon dioxide layer;

forming a silicon nitride on the first silicon dioxide layer; and

forming a second silicon dioxide layer on the silicon nitride layer.

6. The method of claim 5 wherein an upper surface of the first silicon dioxide layer is above the upper surface of the first and second spacers.

7. The method of claim 5 wherein an upper surface of the first silicon dioxide layer is below the upper surface of the first and second spacers and an upper surface of the silicon nitride layer is above the upper surface of the first and second spacers.

8. The method of claim 1 further comprising:

forming a first polysilicon layer during the formation of the first conductive layer and forming a second polysilicon layer during the formation of the second conductive layer;

during the formation of the silicide layer:

forming a metal layer selected from the group consisting of cobalt and nickel on the first and second polysilicon layers and on a portion of the first and second spacers;

heating the metal layer to react the metal layer with the first and second polysilicon layers to form a metal silicide layer from the metal layer and the first and second polysilicon layers, wherein the metal layer on the portion of the first and second spacers remains unreacted; then

subjecting the silicide layer and the unreacted metal layer to an etch which removes the unreacted metal layer and leaves at least a majority of the metal silicide layer.

9. The method of claim 1 further comprising:

forming the at least one dielectric layer from a layer comprising silicon nitride; and

forming the spacer from aluminum oxide.

10. A method used to form a semiconductor device, comprising:

providing a blanket polysilicon word line layer and at least one dielectric layer on the word line layer;

using a single mask, etching the word line layer and the at least one dielectric layer to define a plurality of transistor word lines;

forming a blanket polysilicon plug layer over the plurality of transistor word lines and over the at least one dielectric layer;

planarizing the blanket polysilicon plug layer to remove the plug layer from over the plurality of transistor word lines to form a plurality of polysilicon plugs and to expose the at least one dielectric layer;

subsequent to forming the plurality of polysilicon plugs, using an etch selective to polysilicon to remove the at least one dielectric layer from over the plurality of transistor word lines and to expose the plurality of transistor word lines; and

forming a self-aligned silicide layer which simultaneously forms on the plurality of transistor word lines and on the plurality of plugs.

11. The method of claim 10 further comprising:

subsequent to etching the word line layer and the at least one dielectric layer, forming a plurality of dielectric spacers on the plurality of transistor word lines;

during the removal of the at least one dielectric layer from over the plurality of transistor word lines, exposing a portion of each the dielectric spacer;

forming a metal layer on the plurality of plugs, on the plurality of transistor word lines, and on the exposed portion of each dielectric spacer;

reacting the metal layer with the plurality of transistor word lines and the plurality of plugs to form a metal silicide layer on the plurality of transistor word lines and the plurality of plugs, wherein subsequent to reacting the metal layer with the plurality of transistor word lines and the plurality of plugs, the metal layer on the exposed portion of each dielectric spacer remains unreacted; and

etching the unreacted metal layer with an etch selective to the silicide layer such that subsequent to etching the unreacted metal layer at least a majority of the silicide layer remains.

12. The method of claim 11 further comprising:

forming a first sidewall and a second sidewall from the word line layer and the at least one dielectric layer during the etch of the word line layer and the at least one dielectric layer; and

forming the plurality of dielectric spacers on the plurality of transistor word lines, wherein the first and second sidewalls extend beyond an upper surface of each sidewall.

13. The method of claim 12 further comprising:

exposing a vertically-oriented portion of each sidewall during the removal of the at least one dielectric layer; and

forming the metal layer on the vertically-oriented portion of each sidewall during the formation of the metal layer.

14. The method of claim 11 further comprising forming the dielectric spacers from aluminum oxide.

15. A method used to form a semiconductor device, comprising:

forming a blanket conductive transistor word line layer over a semiconductor wafer substrate assembly;

forming a blanket dielectric layer on the transistor word line layer;

forming a patterned mask over the blanket dielectric layer and over the blanket conductive transistor word line layer;

patterning the blanket dielectric layer and the blanket conductive transistor word line layer using the patterned mask to form a patterned dielectric layer from the blanket dielectric layer and a plurality of transistor word lines from the blanket conductive word line layer;

forming a blanket conductive plug layer over the patterned dielectric layer, over the transistor word lines, and between adjacent transistor word lines;

removing a portion of the blanket conductive plug layer by planarizing the blanket conductive plug layer in the absence of a mask layer to form a plurality of conductive plugs;

subsequent to planarizing the blanket conductive plug layer, removing the patterned dielectric layer in the absence of a mask layer to expose the plurality of transistor word lines;

subsequent to removing the patterned dielectric layer, forming a blanket metal layer on the plurality of conductive plugs, the plurality of transistor word lines, and on exposed dielectric layers;

converting the metal layer on the conductive plugs and on the transistor word lines to an enhancement layer, while the metal layer on the exposed dielectric layers remains unconverted; and

removing the unconverted portion of the metal layer in the absence of a mask layer and leaving the enhancement layer.

16. The method of claim 15 further comprising forming a first silicon dioxide layer, a silicon nitride layer, and a second silicon dioxide layer during the formation of the blanket dielectric layer.

17. The method of claim 15 further comprising:

forming first and second dielectric spacers on the patterned dielectric layer and on the transistor word lines such that an inside surface of each spacer contacts the patterned dielectric layer, and wherein the patterned dielectric layer extends above a top of each of the first and second dielectric spacers;

exposing the inside surface of each of the first and second spacers during the removal of the patterned dielectric layer;

during the formation of the blanket metal layer, forming the blanket metal layer on the inside surface of each of the first and second spacers; and

removing the metal layer from the inside surface of each of the first and second spacers during the removal of the unconverted portion of the metal layer in the absence of the mask.

18. An in-process semiconductor device comprising:

a word line comprising first and second vertically-oriented surfaces and a horizontally-oriented surface interposed between the first and second vertically-oriented surfaces;

first and second spacers, each spacer comprising a vertically-oriented surface having a first portion which contacts the word line and a second portion which is exposed; and

first and second conductive plugs each comprising a first exposed surface which forms a generally continuous vertically-oriented surface with the second portion of one of the spacers, and each plug further comprising a second surface which contacts the spacer with which its first exposed surface forms the continuous vertically-oriented surface.

19. A dynamic random access memory device comprising:

first and second conductive plugs each having a horizontally-oriented surface and a vertically-oriented surface;

a conductive transistor control gate interposed between the first and second conductive plugs, the conductive transistor control gate having first and second vertically-oriented surfaces and a horizontally-oriented surface;

first and second dielectric spacers each having a top surface and first and second vertically-oriented surfaces, wherein the first vertically-oriented surface of the first and second dielectric spacers each contact one of the first and second vertically-oriented surfaces of the conductive transistor control gate, and the second vertically-oriented surface of the first and second dielectric spacers each contact the vertically-oriented surface of one of the first and second conductive plugs, and the top surface of each spacer is above the horizontally-oriented surface of the conductive transistor control gate; and

a conductive layer comprising a first portion formed on the horizontally-oriented surface of the conductive transistor control gate which contacts the first vertically-oriented surface of the first and second dielectric spacers and further comprising a second portion formed on the horizontally-oriented surface of each the conductive plug.

20. The dynamic random access memory device of claim 19 further comprising a dielectric layer which contacts the first and second portions of the conductive layer, the first and second spacers, and which contacts neither the first and second plugs nor the transistor control gate.